Dai-Rong Wu

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CAD Engineer | PDK Development | EDA Workflow Automation | Device Modeling Engineer

PROFESSIONAL SUMMARY

CAD/PDK and device modeling engineer with 7+ years of cross-national experience in semiconductor and EDA automation. Proven expertise in SPICE modeling, PDK development, and CAD tool integration. Adept at Python, Cadence SKILL, and automation across Virtuoso. Experience with traditional nodes and FinFET technology nodes PDK development.

Green card in progress: NIW I-140 approved; requires visa sponsorship before priority date becomes current.

CORE SKILLS

- **EDA Tools:** Cadence Virtuoso(Schematic/Layout Editor, ADE), Siemens Tanner, Mentor Graphics Calibre (DRC/LVS/PEX)
- **Programming:** Cadence SKILL, Python, C++, Tcl, Perl, Verilog, Shell
- **PDK/iPDK:** PCell development, CDF, Callbacks, Netlisting, DRC/LVS deck file generation, testbench development.
- **Modeling:** SPICE Models (BSIM4, BSIM-Bulk, HiSIM-HV), Reliability and RF Modeling, Simulators(HSPICE, Spectre, Eldo)
- **Workflow:** SVN, Git (version control), Jira (issue tracking), Confluence (documentation)
- **Semiconductor Expertise:** CMOS, Finfet, High-Voltage Devices, VLSI Design, Device Characterization

PROFESSIONAL EXPERIENCE

Staff Engineer - Compact Modeling Engineer | Infineon Technologies, Germany | Sep 2023 - Present

- Performed on-wafer measurements and extracted the characteristics of power devices, developed and validated SPICE models across multiple simulators with on-time delivery and good model quality
- Led cross-functional collaboration with foundry partners and internal teams for SPT9U technology enablement, cooperated with international teams and assisted the design team regarding PDK/models.

Software Engineer - EDA Development | Siemens EDA, Taiwan | Mar 2020 - Aug 2023

- Developed PDKs for **5+** foundries across **10+** process nodes, enabling seamless integration with Tanner
- Spearheaded TSMC iPDK conversion project, delivering iPDK that cut development time by 50%

Senior Engineer - Device Modeling | UMC, Taiwan | Jan 2018 - Mar 2020

- Built **10+** comprehensive SPICE models for MOSFETs, diodes, varactors, resistors, and RF devices
- Mentored colleagues in modeling tasks and EDA tools usage, building team capability and knowledge transfer

KEY ACHIEVEMENTS & PROJECTS

Virtuoso-Integrated Automation Script| *Infineon Technologies*

- Developed an automation tool integrated with Virtuoso including testbench generation, simulation and reporting
- Impact: Adopted by 3 technologies, reduced QA cycle time by **88% (12h → 1.5h)** and automated manual processes

Parameter Extraction Tool with Gradient-Based Optimization

- GUI-based semi-automated parameter centering tool using gradient descent optimization to minimize error
- Impact: Reduced manual centering time **by 93%**, accelerating SPICE model tuning and delivery

iPDK Development Project| Siemens EDA

- Led end-to-end development of TSMC iPDK conversion enabling cross-platform compatibility
- Impact: **50%** development time reduction by automation scripts and optimized QA flow

EDUCATION

Master of Science in Electronics | National Chiao Tung University, Taiwan | 2015-2017

1st Author Publications:

- *Crosstalk between single-photon avalanche diodes in a 0.18 μm high-voltage CMOS process. Journal of Lightwave Technology*
- *Time-Correlated Crosstalk Measurements Between CMOS Single-Photon Avalanche Diodes. 2018 International Conference on OMN*

Bachelor of Science in Physics | National Taiwan Normal University, Taiwan | 2011-2015

ADDITIONAL INFORMATION

Certification: Cadence Advanced SKILL Language Programming, SKILL Development of Parameterized Cells

Language: English (Fluent), German (A2), Mandarin (Native), Taiwanese (Native)

U.S. Green Card in Progress: EB-2 NIW I-140 approved, awaiting priority date, requires VISA sponsorship